15-4-4/2

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 3/15/2004 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, JEF-4B68, 272-2511.

Date 5/25/05 Serial # 10/696,632 Priority Application Date 10/29/03

Your Name Thanhha Pham Examiner # 77023

AU 2813 Phone 2-1696 Room Jeff 7C79

In what format would you like your results? Paper is the default. PAPER DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other:

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements.

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ✓ Other

Secondary Refs ✓ Foreign Patents ✓

Teaching Refs ✓

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Test structure for electrical evaluation

- souce/drain electrode → Al, Er, Gd, Nd, Ti, Y, Ag, Au, Al, Cr, Cu, Mg, Pt
- SOI, SSGOI, Silion or semiconductor on Insulator

Staff Use Only

Searcher: Steenkard

Searcher Phone:

Searcher Location: STIC-EIC2800, JEF-4B68

Date Searcher Picked Up: 5/25/05

Date Completed: 5/25/05

Searcher Prep/Rev Time: 30

Online Time: 90

Type of Search

Structure (#)

Bibliographic ✓

Litigation

Fulltext ✓

Patent Family ✓

Other

Vendors

STN ✓

Dialog

QuestelOrbit ✓

Lexis-Nexis

WWW/Internet

Other

Query/Command : HIS

File : PLUSPAT

SS	Results		
1		1	US20050092985/PN
2		1	(I) ..FAM US20050092985/PN
3		2	..CITF US20030107376/PN
4		2	..CITF US20030107376/PN
5		1	..CITB US20050092985/PN

FAMILY CITATION SEARCH

Search statement 6

Query/Command : PRT MAX SET

1 / 1 PLUSPAT - ©QUESTEL-ORBIT - image

PN - US2005092985 A1 20050505 [US20050092985]

TI - (A1) Single and double-gate pseudo-fet devices for semiconductor materials evaluation

LA - ENGLISH (ENG)

PA - (A1) IBM (US)

PA0 - INTERNATIONAL BUSINESS MACHINES CORPORATION; ARMONK, NY [US]

IN - (A1) HOVEL HAROLD J (US); MCKOY THERMON E (US)

AP - US69663203 20031029 [2003US-0696632]

PR - US69663203 20031029 [2003US-0696632]

IC - (A1) G01R-031/26 H01L-021/00 H01L-021/66 H01L-021/8234 H01L-023/58 H01L-029/10

PCL - ORIGINAL (O) : 257048000; CROSS-REFERENCE (X) : 438014000; 438018000; 438197000; 257288000

DT - Basic

STG - (A1) Utility Patent Application published on or after January 2, 2001

AB - Several methods and structures are disclosed for determining electrical properties of silicon-on-insulator (SOI) wafers and alternate versions of such wafers such as strained silicon:silicon/germanium:-on-insulator (SSGOI) wafers. The analyzed electrical properties include mobilities, interface state densities, and oxide charge by depositing electrodes on the wafer surface and measuring the current-voltage behavior using these electrodes. In a single gate structure, the source and drain electrodes reside on the wafer surface and the buried insulator acts as the gate oxide, with the substrate acting as the gate electrode. In a double gate structure, an oxide is used on the upper surface between the source and drain electrodes and an additional metal layer is used on top of this oxide to act as a second gate electrode. Light of broad spectrum or specific wavelength may be used to alter electrical carrier densities in the region between the electrodes to further analyze the electrical properties of the material, or alternatively, the device can be used as a detector of light having a wavelength shorter than the bandgap wavelength of the Si surface.

UP - 2005-18

Search statement 3

Query/Command : PRT MAX SET

1 / 2 PLUSPAT - ©QUESTEL-ORBIT - image

PN - US2004070397 A1 20040415 [US20040070397]
PN2 - US6798204 B2 20040928 [US6798204]
TI - (A1) Manufacturing technique for local MRI coil using metal foil construction
PA - (B2) IGC MEDICAL ADVANCES INC (US)
PA0 - IGC - Medical Advances, Inc., Milwaukee WI [US]
PA2 - (B2) IGC MEDICAL ADVANCES INC (US)
IN - (A1) PIKELJA VELIBOR (US); SEEBER DEREK (US)
AP - US26833902 20021009 [2002US-0268339]
PR - US26833902 20021009 [2002US-0268339]
IC - (A1) G01V-003/00
EC - G01R-033/341
ICO - S01R-033/34F
PCL - ORIGINAL (O) : 324318000; CROSS-REFERENCE (X) : 324322000
DT - Basic
CT - Cited; US5568051; US6060882; US6194900; US6215307; US6259251; US6263229; US6437567; US6556012; US6580274; US6633161; US20010022515; US20030107376; US20040070397
STG - (A1) Utility Patent Application published on or after January 2, 2001
STG2 - (B2) U.S. Patent (with pre-grant pub.) after Jan. 2, 2001
AB - A local coil for magnetic resonance imaging equipment employs mirror conductors on opposite sides of an insulating substrate to produce lower resistance, higher Q and improved signal-to-noise ratio for a given foil thickness.
UP - 2004-17

2 / 2 PLUSPAT - ©QUESTEL-ORBIT - image

PN - US2003107376 A1 20030612 [US20030107376]
PN2 - US6859035 B2 20050222 [US6859035]
TI - (A1) Magnetic resonance imaging apparatus
PA - (A1) TSOHIBA KK (US)
PA0 - Kabushiki Kaisha Toshiba, Kawasaki [JP]
PA2 - (B2) TOKYO SHIBAURA ELECTRIC CO (JP)

IN - (A1) YASUHARA YASUTAKE (JP)

AP - US30372002 20021126 [2002US-0303720]

FD - Divsn of US09764221 20010119 [2001US-0764221]
Division of: US6556012

PR - US30372002 20021126 [2002US-0303720]
JP2000013234 20000121 [2000JP-0013234]
JP2000029601 20000207 [2000JP-0029601]
JP2000305060 20001004 [2000JP-0305060]
JP2000400361 20001228 [2000JP-0400361]
US76422101 20010119 [2001US-0764221]

IC - (A1) G01V-003/00

EC - G01R-033/385
G01R-033/385F

DT - Corresponding document

CT - Cited; US4672346; US5007425; US5124651; US5210494; US5278502; US5663646; US6469507; Cited; US4652824; US5053711; US5361763; US5404882; US5489848; US5764059; US5793210; US6022195; US6043653; US6157276; US6353319; US6406427; US6437568; US6441614; JP61-197321; JP9-149893
Cited by applicant
Katsunuma et al, "Silent MRI System by interrupting the Vibrational Transmission Through the Air and Solid Structures", ISMRM, 1372, 2000.

STG - (A1) Utility Patent Application published on or after January 2, 2001

STG2 - (B2) U.S. Patent (with pre-grant pub.) after Jan. 2, 2001

AB - A magnetic resonance imaging apparatus generates an MR signal from an object to be examined by applying a gradient field pulse generated by a gradient field coil and a high-frequency magnetic field pulse generated by a high-frequency coil to the object in a static field generated by a static field magnet, and reconstructs an image on the basis of the MR signal. The gradient field coil is housed in a sealed vessel. Numerous techniques are disclosed to reduce adverse effects of vibrations caused by rapidly changing gradient coil currents. By judicious use of non-conducting connection components between gantry components at some joint portions requiring electrical contact and at some other portions not requiring electrical contact, the generation of adverse B waves, and/or induced electron flow in response to physical vibration between joint components can be reduced.

UP - 2003-25

```
     (FILE 'HOME' ENTERED AT 15:31:48 ON 25 MAY 2005)

     FILE 'REGISTRY' ENTERED AT 15:32:01 ON 25 MAY 2005
L1           51 SEA ABB=ON  PLU=ON  AL/MF
L2          195 SEA ABB=ON  PLU=ON  ER/MF
L3          233 SEA ABB=ON  PLU=ON  GD/MF
L4          226 SEA ABB=ON  PLU=ON  ND/MF
L5          120 SEA ABB=ON  PLU=ON  TI/MF
L6          125 SEA ABB=ON  PLU=ON  Y/MF
L7          950 SEA ABB=ON  PLU=ON  (L1 OR L2 OR L3 OR L4 OR L5 OR L6)
L8          175 SEA ABB=ON  PLU=ON  AG/MF
L9           51 SEA ABB=ON  PLU=ON  AL/MF
L10         208 SEA ABB=ON  PLU=ON  AU/MF
L11         108 SEA ABB=ON  PLU=ON  CR/MF
L12         133 SEA ABB=ON  PLU=ON  CU/MF
L13          83 SEA ABB=ON  PLU=ON  MG/MF
L14         146 SEA ABB=ON  PLU=ON  NI/MF
L15         205 SEA ABB=ON  PLU=ON  PT/MF
L16        1109 SEA ABB=ON  PLU=ON  (L8 OR L9 OR L10 OR L11 OR L12 OR L13 OR
                L14 OR L15)

     FILE 'HCAPLUS' ENTERED AT 15:36:07 ON 25 MAY 2005
L*** DEL2013752 S L7 OR (AL OR ALUMINIUM OR ER OR ERBIUM OR GD OR GADOLINIUM OR
L17     1020301 SEA ABB=ON  PLU=ON  L7 OR (ALUMINIUM OR ERBIUM OR GADOLINIUM
                OR NEODYMIUM OR TITANIUM OR YTTRIUM)
L18     2581537 SEA ABB=ON  PLU=ON  L16 OR (SILVER OR ALUMINIUM OR GOLD OR
                CHROMIUM OR COPPER OR MAGNESIUM OR NICKEL OR PLATINUM)
L19      604438 SEA ABB=ON  PLU=ON  L17 AND L18
L20         999 SEA ABB=ON  PLU=ON  L19 AND (SOURCE OR DRAIN)(2A)ELECTROD?
L21          15 SEA ABB=ON  PLU=ON  L20 AND (SOI OR SSGOI OR (SILICON OR
                SI)(1W)SEMICONDUCT?(1W)INSULAT? OR  (SI OR SILICON)(1W)((SI OR
                SILICON)(1W)(GERMANIUM OR GE) OR SIGE)(1W)INSULAT?)
                D BIB AB HITSTR
                D BIB AB HITSTR TOT
L22          984 SEA ABB=ON  PLU=ON  L20 NOT L21
L23           79 SEA ABB=ON  PLU=ON  L22 AND (MOS OR METAL(W)OXIDE(1W)SEMICONDUC
                T? OR NMOS OR N(W)MOS OR PMOS OR P(W)MOS OR VMOS OR V(W)MOS OR
                C(W)MOS OR CMOS OR NMOSFET OR NMOS(W)FET  FOR PMOS(W)FET OR
                PMOSFET )
L24           22 SEA ABB=ON  PLU=ON  L23 AND (DMOS(W)FET OR DMOSFET OR UMOS(W)FE
                T OR UMOSFET OR MOS(W)FET OR MOSFET)
L25           13 SEA ABB=ON  PLU=ON  L24 AND (SUBSTRAT? OR SURFACE? OR BASE? OR
                SUBSTRUCT? OR UNDERSTRUCT? OR UNDERLAY? OR FOUNDATION? OR
                PANE? OR DISK? OR DISC? OR WAFER? )
                D BIB AB HITSTR TOT
L26            9 SEA ABB=ON  PLU=ON  L24 NOT L25
L27            0 SEA ABB=ON  PLU=ON  L26 AND ((MONITOR? OR MEASUR? OR TEST? OR
                CHECK? OR EXAMIN? OR ANALYS? OR ANALYZ? OR VERIF? OR IDENTIF?
                OR DETECT? OR SENSE? OR SENSING? OR INSPECT? OR ESTIMAT? OR
                QUANTIF? OR QUANTITAT? OR CALCULAT?)(2A)ELECTRICAL?)
                D L26 BIB AB HITSTR TOT
L28           57 SEA ABB=ON  PLU=ON  L23 NOT L24
L29            0 SEA ABB=ON  PLU=ON  L28 AND (MONITOR? OR MEASUR? OR TEST? OR
                CHECK? OR EXAMIN? OR ANALYS? OR ANALYZ? OR VERIF? OR IDENTIF?
                OR DETECT? OR SENSE? OR SENSING? OR INSPECT? OR ESTIMAT? OR
                QUANTIF? OR QUANTITAT? OR CALCULAT?)(2A)ELECTRICAL?
L30           43 SEA ABB=ON  PLU=ON  L28 AND (SUBSTRAT? OR SURFACE? OR BASE? OR
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SUBSTRUCT? OR UNDERSTRUCT? OR UNDERLAY? OR FOUNDATION? OR PANE? OR DISK? OR DISC? OR WAFER?)

L31 0 SEA ABB=ON PLU=ON S43 AND (SOI OR SSGOI OR (SILICON OR SI)(1W)SEMICONDUCT?(1W)INSULAT? OR (SI OR SILICON)(1W)((SI OR SILICON)(1W)(GERMANIUM OR GE) OR SIGE)(1W)INSULAT?)

D BIB AB HITSTR TOT L30 1-10

D HISL25-

D BIB AB HITSTR TOT L30 11-43

L21 ANSWER 1 OF 15 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2005:394383 HCAPLUS
TI Ultra-shallow junction MOSFET having a high-k gate dielectric and in-situ doped selective epitaxy source/drain extensions and a method of making same
IN Wang, Chih-Hao; Chen, Shang-Chih; Wang, Yen-Ping; Chiu, Hsien-Kuang; Yao, Liang-Gi; Hu, Chenming
PA Taiwan
SO U.S. Pat. Appl. Publ., 15 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2005093084	A1	20050505	US 2004-872095	20040618
PRAI US 2003-516500P	P	20031031		

AB A MOSFET includes a gate having a high-k gate dielec. on a substrate and a gate electrode on the gate dielec. The gate dielec. protrudes beyond the gate electrode. A deep source and drain having shallow extensions are formed on either side of the gate. The deep source and drain are formed by selective in-situ doped epitaxy or by ion implantation and the extensions are formed by selective, in-situ doped epitaxy. The extensions lie beneath the gate in contact with the gate dielec. The material of the gate dielec. and the amount of its protrusion beyond the gate electrode are selected so that epitaxial procedures and related procedures do not cause bridging between the gate **electrode** and the **source** /drain extensions. Methods of fabricating the MOSFET are described.

=> D BIB AB HITSTR TOT

L21 ANSWER 1 OF 15 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2005:394383 HCAPLUS
TI Ultra-shallow junction MOSFET having a high-k gate dielectric and in-situ doped selective epitaxy source/drain extensions and a method of making same
IN Wang, Chih-Hao; Chen, Shang-Chih; Wang, Yen-Ping; Chiu, Hsien-Kuang; Yao, Liang-Gi; Hu, Chenming
PA Taiwan
SO U.S. Pat. Appl. Publ., 15 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2005093084	A1	20050505	US 2004-872095	20040618
PRAI US 2003-516500P	P	20031031		

AB A MOSFET includes a gate having a high-k gate dielec. on a substrate and a gate electrode on the gate dielec. The gate dielec. protrudes beyond the gate electrode. A deep source and drain having shallow extensions are formed on either side of the gate. The deep source and drain are formed by selective in-situ doped epitaxy or by ion implantation and the extensions are formed by selective, in-situ doped epitaxy. The extensions lie beneath the gate in contact with the gate dielec. The material of the gate dielec. and the amount of its protrusion beyond the gate electrode are

selected so that epitaxial procedures and related procedures do not cause bridging between the gate **electrode** and the **source** /drain extensions. Methods of fabricating the MOSFET are described.

L21 ANSWER 2 OF 15 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2005:394337 HCAPLUS
TI Single and double-gate pseudo-FET devices for semiconductor materials evaluation
IN Hovel, Harold J.; McKoy, Thermon E.
PA International Business Machines Corporation, USA
SO U.S. Pat. Appl. Publ., 19 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2005092985	A1	20050505	US 2003-696632	20031029
PRAI US 2003-696632		20031029		

AB In the present invention, no ion implantation or high temperature annealing are used, and no photolithog. is required, although one simple photolithog. step can be used to optimize the device if desired. Several methods and structures are disclosed for determining elec. properties of Si-on-insulator (**SOI**) wafers and alternate versions of such wafers such as strained **Si:Si/Ge:-on-insulator** (**SSGOI**) wafers. The analyzed elec. properties include mobilities, interface state densities, and oxide charge by depositing electrodes on the wafer surface and measuring the current-voltage behavior using these electrodes. In a single gate structure, the **source** and **drain electrodes** reside on the wafer surface and the buried insulator acts as the gate oxide, with the substrate acting as the gate electrode. In a double gate structure, an oxide was used on the upper surface between the **source** and **drain electrodes** and an addnl. metal layer was used on top of this oxide to act as a 2nd gate electrode. Light of broad spectrum or specific wavelength may be used to alter elec. carrier densities in the region between the electrodes to further analyze the elec. properties of the material, or alternatively, the device can be used as a detector of light having a wavelength shorter than the bandgap wavelength of the Si surface.

IT **7429-90-5**, Aluminum **7440-00-8**, **Neodymium** **7440-02-0**, **Nickel** **7440-06-4**, **Platinum** **7440-22-4**, **Silver** **7440-32-6**, **Titanium** **7440-47-3**, **Chromium** **7440-50-8**, **Copper** **7440-52-0**, **Erbium** **7440-54-2**, **Gadolinium** **7440-57-5**, **Gold** **7440-65-5** , **Yttrium**
RL: DEV (Device component use); USES (Uses)
(single and double-gate pseudo-FET devices for **SOI** semiconductor materials elec. property evaluation)

RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

RN 7440-00-8 HCAPLUS
CN Neodymium (8CI, 9CI) (CA INDEX NAME)

Nd

RN 7440-02-0 HCAPLUS
CN Nickel (8CI, 9CI) (CA INDEX NAME)

Ni

RN 7440-06-4 HCAPLUS
CN Platinum (8CI, 9CI) (CA INDEX NAME)

Pt

RN 7440-22-4 HCAPLUS
CN Silver (8CI, 9CI) (CA INDEX NAME)

Ag

RN 7440-32-6 HCAPLUS
CN Titanium (8CI, 9CI) (CA INDEX NAME)

Ti

RN 7440-47-3 HCAPLUS
CN Chromium (8CI, 9CI) (CA INDEX NAME)

Cr

RN 7440-50-8 HCAPLUS
CN Copper (7CI, 8CI, 9CI) (CA INDEX NAME)

Cu

RN 7440-52-0 HCAPLUS
CN Erbium (8CI, 9CI) (CA INDEX NAME)

Er

RN 7440-54-2 HCAPLUS
CN Gadolinium (8CI, 9CI) (CA INDEX NAME)

Gd

RN 7440-57-5 HCAPLUS
CN Gold (8CI, 9CI) (CA INDEX NAME)

Au

RN 7440-65-5 HCAPLUS
CN Yttrium (8CI, 9CI) (CA INDEX NAME)

Y

L21 ANSWER 3 OF 15 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2005:371528 HCAPLUS
DN 142:421841
TI Dynamic Schottky barrier MOSFET device and method of manufacture
IN Snyder, John P.; Larson, John M.
PA Spinnaker Semiconductor, Inc., USA
SO PCT Int. Appl., 49 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 2005038901	A1	20050428	WO 2004-US34686	20041021
W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW				
RW: BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG				
PRAI US 2003-513410P	P	20031022		
US 2003-514041P	P	20031024		

AB A device for regulating a flow of elec. current and its manufacturing method are provided. The device includes metal-insulator-semiconductor (MOS) source-drain contacts forming Schottky barrier or Schottky-like junctions to the semiconductor substrate. The device includes an interfacial layer between the semiconductor substrate and a metal source and/or **drain electrode**, thereby dynamically adjusting a Schottky barrier height by applying different bias conditions. The dynamic Schottky barrier modulation provides increased elec. current for low drain bias conditions, reducing the sub-linear turn-on characteristic of Schottky barrier MOSFET devices and improving device performance.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L21 ANSWER 4 OF 15 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2004:1059009 HCAPLUS
DN 142:47235
TI Field effect transistor using vanadium dioxide layer as channel material to control a large current even in devices having small areas
IN Kim, Hyun Tak; Kang, Kwang Yong; Youn, Doo Hyeb; Chae, Byung Gyu
PA S. Korea
SO U.S. Pat. Appl. Publ., 7 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2004245582	A1	20041209	US 2003-749596	20031230
PRAI	KR 2003-35556	A	20030603		

AB The present invention provides a field effect transistor which induces a sharp metal-insulator transition by adding low-d. holes to a vanadium dioxide thin film to control a large current even in devices having small areas. The field effect transistor includes an insulating vanadium dioxide (VO2) thin film used as a channel material, a **source electrode** and a **drain electrode** disposed on the insulating VO2 thin film to be spaced apart from each other by a channel length, a dielec. layer disposed on the **source electrode**, the **drain electrode**, and the insulating VO2 thin film, and a gate electrode for applying a predetd. voltage to the dielec. layer.
IT **7440-47-3, Chromium**, uses **7440-57-5, Gold**, uses
RL: DEV (Device component use); USES (Uses)
(**source/drain/gate electrode**; field effect transistor using vanadium dioxide layer as channel material to control large current even in devices having small areas)
RN 7440-47-3 HCAPLUS
CN Chromium (8CI, 9CI) (CA INDEX NAME)

Cr

RN 7440-57-5 HCAPLUS
CN Gold (8CI, 9CI) (CA INDEX NAME)

Au

L21 ANSWER 5 OF 15 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2004:1037405 HCAPLUS
DN 142:47147
TI Field effect transistor using insulator-semiconductor transition material layer as channel material and method of manufacturing the same
IN Kim, Hyun-Tak; Kang, Kwang-Yong; Youn, Doo-Hyeb; Chae, Byung-Gyu
PA Electronics and Telecommunications Research Institute, S. Korea
SO PCT Int. Appl., 17 pp.
CODEN: PIXXD2

DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 2004105139	A1	20041202	WO 2003-KR2893	20031230

W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW

RW: BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG

PRAI KR 2003-31903 A 20030520

AB Provided is a field effect transistor including an insulator-semiconductor transition material layer. The insulator-semiconductor transition material layer selectively provides a 1st state where charged holes are not introduced to a surface of the insulator-semiconductor transition material layer when a gate field is not applied and a 2nd state where a large number of charged holes are introduced to the surface of the insulator-semiconductor transition material layer to form a conductive channel when a neg. field is applied. A gate insulating layer is formed on the insulator-semiconductor transition material layer. A gate electrode is formed on the gate insulating layer to apply a neg. field of a predetd. intensity to the insulator-semiconductor transition material layer. A **source electrode** and a **drain electrode** are disposed to face each other at both sides of the insulator-semiconductor transition material layer so that charge carriers can flow through the conductive channel while the insulator-semiconductor transition material layer is in the 2nd state.

IT **7440-47-3, Chromium**, uses **7440-57-5, Gold**, uses
RL: DEV (Device component use); USES (Uses)
(electrodes; field effect transistor using insulator-semiconductor transition material layer as channel material and method of manufacturing the same)

RN 7440-47-3 HCAPLUS
CN Chromium (8CI, 9CI) (CA INDEX NAME)

Cr

RN 7440-57-5 HCAPLUS
CN Gold (8CI, 9CI) (CA INDEX NAME)

Au

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L21 ANSWER 6 OF 15 HCAPLUS COPYRIGHT 2005 ACS on STN

AN 2002:696399 HCAPLUS
DN 137:225340
TI Semiconductor device having silicon-on-insulator structure and method of fabricating the same
IN Kim, Min-su; Kim, Kwang-il
PA Samsung Electronics Co., Ltd., S. Korea
SO U.S. Pat. Appl. Publ., 14 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002125534	A1	20020912	US 2001-994146	20011126
	KR 2002072675	A	20020918	KR 2001-12630	20010312
	JP 2002289872	A2	20021004	JP 2002-14844	20020123
PRAI	KR 2001-12630	A	20010312		

AB A semiconductor device having a silicon-on-insulator (**SOI**) structure is provided. The semiconductor device includes: an insulating layer; an insular silicon region having first conductive impurity ions and being formed on the insulating layer; a source region having second conductive impurity ions and being formed at an end of the insular silicon region; a drain region having second conductive impurity ions and spaced apart from the source region at the other end of the insular silicon region; an insular body region which is disposed between the source and drain regions and on which a channel is formed; a body contact region having first conductive impurity ions and being connected to the source region and the insular body region; a conductive layer formed on the source region and the body contact region; and a **source electrode** in contact with the body contact region on the source region.

L21 ANSWER 7 OF 15 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2002:461245 HCAPLUS
DN 137:26918
TI Method for forming electrostatic discharge (ESD) protection network for **SOI** technology with ESD device formed in underlying silicon substrate
IN Jun, Song; Ang, Ting Cheong; Loong, Sang Yee; Quek, Shyue Fong
PA Chartered Semiconductor Manufacturing Ltd., Singapore
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6406948	B1	20020618	US 2000-615807	20000713
	SG 101456	A1	20040130	SG 2001-4141	20010711
	US 2002115239	A1	20020822	US 2002-131536	20020424
	US 6486515	B2	20021126		
PRAI	US 2000-615807	A	20000713		

AB A method for forming an ESD device using silicon-on-insulator (**SOI**) technol. is described. An N-well is formed within a silicon semiconductor substrate. A P+ region is implanted within a portion of the N-well, and an N+ region is implanted within a portion of the semiconductor substrate not occupied by the N-well. An oxide layer is formed overlying the semiconductor substrate and patterned to form

openings to the semiconductor substrate. An epitaxial silicon layer is grown within the openings and overlying the oxide layer. Shallow trench isolation regions are formed within the epitaxial silicon layer extending to the underlying oxide layer. Gate **electrodes** and associated **source** and drain regions are formed in and on the epitaxial silicon layer between the shallow trench isolation regions. An interlevel dielec. layer is deposited overlying the gate electrodes. First contacts are opened through the interlevel dielec. layer to the underlying source and drain regions. The interlevel dielec. layer is covered with a mask that covers the first contact openings. Second contact openings are opened through the interlevel dielec. layer, shallow trench isolations, and the oxide layer to the N+ region and P+ region. The mask is removed. The first and second contact openings are filled with a conducting layer to complete formation of an ESD device.

IT **7429-90-5**, Aluminum, uses **7440-50-8, Copper,** uses
RL: DEV (Device component use); USES (Uses)
(formation of electrostatic discharge protection network for **SOI** technol. with electrostatic discharge device formed in underlying silicon substrate)
RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

RN 7440-50-8 HCAPLUS
CN Copper (7CI, 8CI, 9CI) (CA INDEX NAME)

Cu

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L21 ANSWER 8 OF 15 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2002:90478 HCAPLUS
DN 136:143746
TI Semiconductor device and method for manufacturing the same
IN Yagishita, Atsushi; Matsuo, Kouji
PA K. K. Toshiba, Japan
SO U.S. Pat. Appl. Publ., 43 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002011613	A1	20020131	US 2001-901721	20010711
	JP 2002094058	A2	20020329	JP 2001-174567	20010608
	TW 497131	B	20020801	TW 2001-90115681	20010628
	CN 1333568	A	20020130	CN 2001-122374	20010711
	US 2002179980	A1	20021205	US 2002-205203	20020726
	US 6887747	B2	20050503		
PRAI	JP 2000-210473	A	20000711		
	JP 2001-174567	A	20010608		

US 2001-901721 A3 20010711

AB A semiconductor device in which isolating insulating film is formed in a periphery of a device region of a semiconductor silicon substrate device region. A side wall insulating film formed of a silicon nitride film is formed to cover the periphery of a channel region on the silicon substrate. A Ta2O5 film, and a metal gate electrode are formed inside a trench whose side wall is formed of the side wall insulating film. An interlayer insulating film is formed on the device isolating insulating film. A Schottky source/drain formed of silicide is formed on the silicon substrate in a bottom portion of the trench whose side wall is formed of the side wall insulating film and interlayer insulating film. A **source/drain electrode** is formed on the Schottky source/drain.

IT **7429-90-5**, Aluminum, uses
RL: DEV (Device component use); USES (Uses)
(semiconductor device and manufacture of same)

RN 7429-90-5 HCAPLUS

CN Aluminum (8CI, 9CI) (CA INDEX NAME)

A1

L21 ANSWER 9 OF 15 HCAPLUS COPYRIGHT 2005 ACS on STN

AN 2002:31863 HCAPLUS

DN 136:94566

TI **SOI** type MOS transistor

IN Murakami, Norio

PA Oki Electric Industry Co., Ltd., Japan

SO U.S. Pat. Appl. Publ., 12 pp.
CODEN: USXXCO

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002003260	A1	20020110	US 2001-865475	20010529
	US 6469349	B2	20021022		
	JP 2002026311	A2	20020125	JP 2000-202224	20000704
	US 2003062573	A1	20030403	US 2002-237061	20020909
	US 6649455	B2	20031118		
PRAI	JP 2000-202224	A	20000704		
	US 2001-865475	A3	20010529		

AB Disclosed is a **SOI** type MOS element excellent in yield, performance and characteristic, easy in manufacture, and low in cost, and a method of manufacturing the same. A **SOI** type MOS transistor structure comprising polysilicon **electrodes** for gate, **source** and drain composed by burying into trench holes, resp. formed in a semiconductor substrate, a gate oxide film formed in the entire inside of the trench hole, N-diffusion layer and N+ diffusion layer formed in the entire inside of the trench holes, and a thick SiO2 film in a trench hole formed in the semiconductor substrate so as to surround the transistor.

IT **7429-90-5**, Aluminum, uses
RL: DEV (Device component use); USES (Uses)
(electrode; **SOI** type MOS element manufacturing)

RN 7429-90-5 HCAPLUS

CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

L21 ANSWER 10 OF 15 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2002:10929 HCAPLUS
DN 136:78290
TI Semiconductor device of nanocryst. insulating film of silicon compds. or other metal oxides, nitrides and oxynitrides
IN Nishiyama, Akira; Koyama, Masato
PA Japan
SO U.S. Pat. Appl. Publ., 23 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002000593	A1	20020103	US 2001-891129	20010626
	JP 2002016063	A2	20020118	JP 2000-193215	20000627
PRAI	JP 2000-193215	A	20000627		

AB Disclosed is a semiconductor device comprising a semiconductor substrate and a circuit element using an insulating film formed on the semiconductor substrate. The insulating film contains a Si compound containing ≥1 element selected from the group consisting of an O and a N, and a metal compound containing a metal other than Si and ≥1 element selected from the group consisting of an O and a N. Nano-crystals are formed in the insulating film. The size of the nano-crystal is small enough to permit observation of a polycryst. ring as a diffraction image when an electron beam having a beam diameter of the nm order is incident in parallel to the insulating film surface.

IT **7429-90-5**, Aluminum, processes **7440-32-6**, **Titanium**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(Al/TiN/Ti wiring layer; semiconductor device of nanocryst. insulating film of silicon compds. or other metal oxides, nitrides and oxynitrides)

RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

RN 7440-32-6 HCAPLUS
CN Titanium (8CI, 9CI) (CA INDEX NAME)

Ti

IT **7440-50-8**, **Copper**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(Cu/TiN/Ti wiring layer; semiconductor device of nanocryst. insulating

film of silicon compds. or other metal oxides, nitrides and oxynitrides)
RN 7440-50-8 HCAPLUS
CN Copper (7CI, 8CI, 9CI) (CA INDEX NAME)

Cu

IT **7440-22-4, Silver,** processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(wiring layer; semiconductor device of nanocryst. insulating film of silicon compds. or other metal oxides, nitrides and oxynitrides)
RN 7440-22-4 HCAPLUS
CN Silver (8CI, 9CI) (CA INDEX NAME)

Ag

L21 ANSWER 11 OF 15 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2002:6391 HCAPLUS
DN 136:78255
TI Method for improving performance of organic semiconductors in bottom electrode structure
IN Dimitrakopoulos, Christos Dimitrios; Kymissis, Ioannis; Purushothaman, Sampath
PA International Business Machines Corp., USA
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6335539	B1	20020101	US 1999-434365	19991105
	US 2002045289	A1	20020418	US 2001-20698	20011029
	US 6569707	B2	20030527		
PRAI	US 1999-434365	A3	19991105		

AB A method for improving the performance of an organic thin film field effect transistor comprising the steps of: (a) forming a transistor structure having patterned **source** and **drain electrodes** ; and (b) treating the patterned **source** and **drain electrodes** with a thiol compound, RSH, in which R is a linear or branched, substituted or unsubstituted, alkyl, alkenyl, cycloalkyl or aromatic containing from .apprx.6 to .apprx.25 C atoms under conditions that are effective in forming a self-assembled monolayer of the thiol compound on the electrodes. Organic thin film transistor structures containing the self-assembled monolayer of the present invention are also disclosed.
IT **7429-90-5,** Aluminum, processes **7440-06-4, Platinum,** processes **7440-32-6, Titanium,** processes **7440-47-3, Chromium,** processes **7440-57-5, Gold,** processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)

(conductive metal compatible in organic TFT; method for improving performance of organic semiconductors in bottom electrode structure)

RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

RN 7440-06-4 HCAPLUS
CN Platinum (8CI, 9CI) (CA INDEX NAME)

Pt

RN 7440-32-6 HCAPLUS
CN Titanium (8CI, 9CI) (CA INDEX NAME)

Ti

RN 7440-47-3 HCAPLUS
CN Chromium (8CI, 9CI) (CA INDEX NAME)

Cr

RN 7440-57-5 HCAPLUS
CN Gold (8CI, 9CI) (CA INDEX NAME)

Au

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L21 ANSWER 12 OF 15 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1999:719110 HCAPLUS
DN 131:331077
TI Semiconductor device with high voltage stability
IN Teshigahara, Akihiko; Asai, Akiyoshi; Onoda, Kunihiro; Itou, Hiroyasu; Abe, Ryuichirou; Sakakibara, Toshio
PA Denso Corp., Japan
SO Ger. Offen., 30 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 19919955	A1	19991104	DE 1999-19919955	19990430
	JP 11312805	A2	19991109	JP 1998-120867	19980430
	JP 3509552	B2	20040322		
	JP 11330383	A2	19991130	JP 1998-138322	19980520

PRAI JP 1998-120867 A 19980430
JP 1998-138322 A 19980520

AB According to the submitted discovery, an island region which is surrounded by trenches is foreseen. The island region is furthermore surrounded by a buffer region with a buffer region contact film. In the island region, a source area is cyclically surrounding a drain region and **source -and-drain electrodes** are foreseen in the source and drain regions. A cyclic auxiliary electrode is in such a way constructed in the **source electrode**, that it extends over the trenches. Accordingly, a potential that is applied to the **source electrode**, can be applied to the auxiliary electrode so that a concentration of an elec. field between the buffer region and the **source electrode** can be diminished. In the fabrication of this semiconductor device, an element of the first semiconductor element and the second semiconductor element are a P-channel MOSFET and the other element of the first semiconductor element and the second semiconductor element are an N-channel MOSFET element.

IT **7429-90-5**, Aluminum, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(semiconductor device with high voltage stability)

RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

L21 ANSWER 13 OF 15 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1995:896457 HCAPLUS
DN 123:304479
TI Semiconductor devices and manufacture thereof
IN Himi, Keimei; Asai, Shoki
PA Nippon Denso Co, Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 07221321	A2	19950818	JP 1994-36486	19940208
PRAI JP 1994-36486		19940208		

AB A double gate **SOI** MOSFET comprises: a heavy metal back gate electrode (W, Ta, Ti or Mo); a poly-Si front gate electrode; a poly-Si front gate electrode; a BPSG interlayer insulator; and a source and a **drain** Al **electrode**, where the manufacturing process employs a self-aligned x-ray lithog. using the front gate electrode as a photomask.

IT **7429-90-5**, Aluminum, uses **7440-32-6**, **Titanium**, uses
RL: DEV (Device component use); USES (Uses)
(double gate **SOI** MOSFET)

RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

RN 7440-32-6 HCAPLUS
CN Titanium (8CI, 9CI) (CA INDEX NAME)

Ti

L21 ANSWER 14 OF 15 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1995:528485 HCAPLUS
DN 122:279884
TI Manufacture of thin film **SOI** semiconductor devices
IN Hisamoto, Masaru; Kusukawa, Kikuo
PA Hitachi Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 06275803	A2	19940930	JP 1993-58811	19930318
PRAI JP 1993-58811		19930318		

AB In manufacture of a thin film channel insulating gate FET without a substrate power supply electrode on the channel substrate having thin film **SOI** structure, a gate electrode and a wiring layer contacting to the impurity diffusion layer comprising of the **source/drain electrodes** are formed on the different side of the substrate. The diffusion layer electrode is formed in self-alignment to the gate electrode.
IT **7429-90-5**, Aluminum, uses
RL: DEV (Device component use); USES (Uses)
(manufacture of thin film **SOI** semiconductor devices)
RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

L21 ANSWER 15 OF 15 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1994:546647 HCAPLUS
DN 121:146647
TI Semiconductor devices with common gate electrode
IN Funaki, Masanori
PA Victor Company Of Japan, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 06013606	A2	19940121	JP 1992-190170	19920625
PRAI JP 1992-190170		19920625		

AB A common gate electrode semiconductor device has Si-on-insulator (**SOI**) structure having ≥ 2 layers of Si. The device

consists of 1st **SOI** layer having 1st conduction type source zone, drain zone, and intrinsic semiconductor type gate zone; a polysilicon gate electrode changing from 2nd type conduction type 2nd **SOI** layer consisting 2nd conduction type **source** and **drain electrode** on 2nd oxidized gate layer. The threshold voltage of the device in controlled.

IT **7429-90-5**, Aluminum, uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(acceptor, in polysilicon doping by implantation, of **SOI** base semiconductor devices)

RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

Al

L30 ANSWER 1 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2004:739900 HCAPLUS
DN 141:252528
TI Method of fabricating a salicided semiconductor device using a dummy dielectric layer between the source/drain and the gate electrode
IN Tseng, Horng-Huei; Lin, Da-Chi; Yang, Kuo-Nan; Hu, Chenming
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S. Pat. Appl. Publ., 14 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2004175907	A1	20040909	US 2003-383711	20030307

PRAI US 2003-383711 20030307

AB A new method is provided for the creation of **CMOS** devices. A sacrificial layer is deposited over a Si **substrate**. This sacrificial layer is instrumental in creating gate spacers and in doing so serves to sep. the gate from the source/drain regions in a self-aligned manner.

IT **7440-06-4**, **Platinum**, processes **7440-32-6**, **Titanium**, processes
RL: CPS (Chemical process); DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in fabricating salicided semiconductor device using dummy dielec. layer between source/**drain** and gate **electrode**)
RN 7440-06-4 HCAPLUS
CN Platinum (8CI, 9CI) (CA INDEX NAME)

Pt

RN 7440-32-6 HCAPLUS
CN Titanium (8CI, 9CI) (CA INDEX NAME)

Ti

L30 ANSWER 2 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2004:21884 HCAPLUS
DN 140:398295
TI Method for manufacture of transistors having metal silicides on **source/drain electrode**
IN Zeng, Honghui
PA World Advanced Integrated Circuits Co., Ltd., Peop. Rep. China
SO Faming Zhuanli Shenqing Gongkai Shuomingshu, 11 pp.
CODEN: CNXXEV
DT Patent
LA Chinese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	CN 1366335	A	20020828	CN 2001-101281	20010117
PRAI	CN 2001-101281		20010117		

AB The method comprises forming a 1st dielec. layer (an oxide layer 50-300 Å thick) on a **substrate**, forming a conductor layer (metal, polysilicon, or polycide layer, 500-3500 Å thick) on the 1st dielec. layer, conducting a pattern transfer procedure to remove part of the 1st dielec. layer and part of the conductor layer to create a gate structure, forming spacer (SiO2, Si3N4, or SiOxNy) on the side wall of the gate structure, doping metal particles (ions, atoms) into the **substrate** , heat treating to form a metal silicide layer on the **substrate**, and removing the unreacted metal particles.

L30 ANSWER 3 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2002:904908 HCAPLUS
DN 137:392075
TI Double-diffusion **MOS** semiconductor devices and fabrication of devices thereof
IN Tsuchiya, Masanobu; Matsuda, Noboru; Kawamura, Keiko; Osawa, Akihiko
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2002343968	A2	20021129	JP 2001-143380	20010514
PRAI	JP 2001-143380		20010514		

AB The title devices comprise (1) a p-type highly-doped semiconductor **substrate**, (2) a p-type lightly-doped epitaxial layer formed on the **substrate**, (3) a p-type 1st diffusion layer provided in a desired position and depth in the epitaxial layer, (4) an n-type 2nd diffusion layer formed inside the 1st diffusion layer, and (5) a metal plug pierced from the top of the diffusion layers through the 1st and 2nd diffusion layers in the epitaxial layer down to the top of the semiconductor **substrate**. The metal plug provides elec. conduction of the source as the n-type 2nd diffusion layer to the **substrate** which is connected to an external wiring sa as to decrease the ON resistance in the horizontal DMOS semiconductor devices.

IT **7429-90-5**, Aluminum, properties **7440-50-8**, **Copper**, properties **7440-57-5**, **Gold**, properties
RL: DEV (Device component use); PRP (Properties); USES (Uses)
(conductive plug; double-diffusion **MOS** semiconductor devices and fabrication of devices thereof)

RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

RN 7440-50-8 HCAPLUS
CN Copper (7CI, 8CI, 9CI) (CA INDEX NAME)

Cu

RN 7440-57-5 HCAPLUS
CN Gold (8CI, 9CI) (CA INDEX NAME)

Au

L30 ANSWER 4 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2002:307670 HCAPLUS
DN 137:55587
TI Field-effect-assisted photoconductivity in PbS films deposited on silicon dioxide
AU Pintilie, L.; Pentia, E.; Matei, I.; Pintilie, I.; Ozbay, E.
CS National Institute of Materials Physics, Bucharest-Magurele, 76900, Rom.
SO Journal of Applied Physics (2002), 91(9), 5782-5786
CODEN: JAPIAU; ISSN: 0021-8979
PB American Institute of Physics
DT Journal
LA English
AB Lead sulfide (PbS) thin films were deposited from a chemical bath onto SiO2/Si (n-type) **substrates**. Pseudo-**metal-oxide-semiconductor** devices were obtained by evaporating source and **drain gold electrodes** on a PbS **surface** and aluminum gate electrode on a Si **substrate**. Field-effect-assisted photocond. in the PbS layer was investigated at room temperature, in the 800-2700-nm-wavelength domain for different values and polarities of the drain and gate voltages. The best results were obtained for a pos. gate, when both semiconductors are in depletion. An enhancement of about 25% of the photoconductive signal is obtained compared with the case when the gate electrode is absent or is not used. A simple model is proposed that explains the behavior of the dark current and photoconductive signal in PbS film with changing the gate voltage.
IT **7429-90-5**, Aluminum, properties
RL: DEV (Device component use); PRP (Properties); USES (Uses)
(field-effect-assisted photocond. in PbS films deposited on silicon dioxide)
RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

RE.CNT 14 THERE ARE 14 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L30 ANSWER 5 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2001:828130 HCAPLUS
DN 135:337941
TI Method for gate-drain multilayer structure by liquid phase deposition of silica layer in **CMOS** fabrication
IN Wu, Shie-Lin
PA Powerchip Semiconductor Corporation, Taiwan
SO Taiwan, 22 pp.

CODEN: TWXXA5
DT Patent
LA Chinese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI TW 383408	B	20000301	TW 1997-86104000	19970328
PRAI TW 1997-86104000		19970328		

AB A method for **CMOS** transistor multilayer gate-drain structure is **disclosed**. A field oxide layer is formed on a semiconductor **substrate**, followed by 1st conductive well, 2nd conductive well, gate electrode and gate oxide layer. A first dielec. layer is formed on top of gate electrode and gate oxide layer to compensate damaged gate oxide layer, followed by a lightly doped **drain electrode** formation in the 1st conductive well and 2nd conductive well. A plurality of amorphous Si sidewall is formed on both sides of the gate electrode, followed by formation of heavily doped **source/drain electrodes** and gate electrodes. A liquid phase deposited silicon oxide sidewall is formed on both sides of amorphous Si sidewall. and metal silicide is formed on **source/drain electrodes** , gate **electrode** and amorphous Si sidewall which are not covered with on liquid phase deposited Si oxide sidewall. Finally, metal silicide is formed on **source/drain electrodes**, gate **electrode** and amorphous Si sidewall which are not covered with on liquid phase deposited Si oxide sidewall.

IT **7429-90-5**, Aluminum, processes
RL: PEP (Physical, engineering or chemical process); RCT (Reactant); PROC (Process); RACT (Reactant or reagent)
(liquid phase deposition; multilayer gate-drain structure by liquid phase deposition of silica layers in **CMOS** fabrication)
RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

L30 ANSWER 6 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2001:823600 HCAPLUS
DN 135:338011
TI Partial formation of anti-short-channel doped area on the source side in **MOS** transistor fabrication
IN Wang, Jau-Jie; Tsai, Jau-Jie; Liou, Jing-Meng
PA Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan
SO Taiwan, 16 pp.
CODEN: TWXXA5
DT Patent
LA Chinese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI TW 381311	B	20000201	TW 1998-87112503	19980729
PRAI TW 1998-87112503		19980729		

AB A **MOS** device is comprised of a semiconductor **substrate** separated from an active area by a spacer, a gate electrode formed in the active area, a channeling area with two ends under the gate **electrode**, a **drain electrode** of first

conductivity-type doped area formed in one end of the channel, a **source electrode** of first conductivity-type on the other end of the channel with a dented area, a bulk contact area of second conductivity-type doped area formed in the dented area of mentioned above, an anti-short-channel doped area of second conductivity-type formed under the channel area close to the above **drain electrode** side as well as to the side of **source electrode** area except the bulk contact area. Therefore, a silicon **substrate** has an effective usage of the **surface** area and increased productivity.

L30 ANSWER 7 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2001:645644 HCAPLUS
DN 135:203938
TI **MOS** transistors having dual gates and self-aligned interconnect contact windows
IN Ni, Cheng-Tsung
PA Mosel Vitelic, Inc., Taiwan
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6284578	B1	20010904	US 2000-534699	20000324
	US 2001049165	A1	20011206	US 2001-896205	20010628
	US 6657263	B2	20031202		
PRAI	TW 1999-88104775	A	19990326		
	US 2000-534699	A3	20000324		

AB A method is presented for fabricating an IC device on a **substrate** comprising **MOS** transistors and other IC components. Each of the transistors of the IC device comprises a raised **source electrode**, a raised **drain electrode**, dual gate electrodes and self-aligned interconnect contact windows, and is connected to other transistors and other IC components through interconnects formed on top of such self-aligned contact windows.
RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L30 ANSWER 8 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2001:581412 HCAPLUS
DN 135:130927
TI Raised silicide source/drain **MOS** transistors and method
IN Sakiyama, Keizo; Hsu, Sheng Teng
PA Sharp K. K., Japan
SO Eur. Pat. Appl., 19 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1122771	A2	20010808	EP 2001-300938	20010202
	EP 1122771	A3	20011128		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	US 6352899	B1	20020305	US 2000-497626	20000203

	JP 2001237427	A2	20010831	JP 2001-27567	20010202
	TW 480604	B	20020321	TW 2001-90102359	20010205
PRAI	US 2000-497626	A	20000203		

AB A method is provided for forming silicided **source/drain electrodes** in active devices in which the electrodes have thin junction regions. In the process, adjacent active areas are separated by isolation regions, typically by local oxidation of Si structure isolation, trench isolation, or Si on insulator/separation by implanted O2 isolation. A contact material, preferably silicide, is deposited over the **wafer** and the underlying structures, including gate and interconnect electrodes. The silicide is then planed away using chemical-mech. polishing, or another suitable planing process, to a height approx. the height of the highest structure. The silicide is then elec. isolated from the electrodes, using an etch back process, or other suitable process, to lower the silicide to a height below the height of the gate or interconnect electrode. The **wafer** is then patterned and etched to remove unwanted silicide. The remaining silicide typically forms silicided source regions and silicided drain regions that extend over a portion of the adjacent isolation regions such that the silicided source/drain regions are larger than the underlying source/drain regions to provide a larger contact area.

IT **7440-02-0, Nickel**, reactions **7440-06-4, Platinum**, reactions **7440-32-6, Titanium**, reactions
RL: RCT (Reactant); RACT (Reactant or reagent)
(silicidation for raised source/drain **MOS** transistors)

RN 7440-02-0 HCAPLUS
CN Nickel (8CI, 9CI) (CA INDEX NAME)

Ni

RN 7440-06-4 HCAPLUS
CN Platinum (8CI, 9CI) (CA INDEX NAME)

Pt

RN 7440-32-6 HCAPLUS
CN Titanium (8CI, 9CI) (CA INDEX NAME)

Ti

L30 ANSWER 9 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2001:277986 HCAPLUS
DN 134:274374
TI Silicide encapsulation of polysilicon gate and interconnect
IN Liu, Yauh-ching; Giust, Gary K.; Castagnetti, Ruggero; Ramesh, Subramanian
PA LSI Logic Corporation, USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6218276	B1	20010417	US 1997-995875	19971222
PRAI	US 1997-995875		19971222		

AB Provided is a method of forming a silicide layer on the top and sidewall **surfaces** of a polysilicon gate/interconnect in a **MOS** transistor and on the exposed **surfaces** of the source and drain regions of the transistor. Devices produced according to the present invention may have different types of silicide formed on their gate and their **source/drain electrodes**. The invention achieves the advantages of silicide encapsulation of a polysilicon gate in an **MOS** transistor while also providing silicidation of the source/drain regions of the transistor, thereby reducing electrode resistivity in the transistor and interconnect.

IT **7440-02-0, Nickel**, processes **7440-32-6, Titanium**, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); RCT (Reactant); PROC (Process); RACT (Reactant or reagent); USES (Uses)
(in silicide encapsulation of polysilicon gate and interconnect)

RN 7440-02-0 HCAPLUS
CN Nickel (8CI, 9CI) (CA INDEX NAME)

Ni

RN 7440-32-6 HCAPLUS
CN Titanium (8CI, 9CI) (CA INDEX NAME)

Ti

RE.CNT 27 THERE ARE 27 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L30 ANSWER 10 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2000:606805 HCAPLUS
DN 133:171117
TI Fabrication of a semiconductor device using self-aligned silicide **CMOS** having dummy gate electrode
IN Ahn, Jae-gyung
PA LG Semicon Co., Ltd., S. Korea
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6110771	A	20000829	US 1999-335048	19990616
	KR 2000019488	A	20000415	KR 1998-37610	19980911
	KR 2000065717	A	20001115	KR 1999-12332	19990408
	US 6373109	B1	20020416	US 2000-604814	20000628
PRAI	KR 1998-37610	A	19980911		
	KR 1999-12332	A	19990408		
	US 1999-335048	A3	19990616		

AB A semiconductor device and a fabrication method therefor improve electrostatic **discharge** (ESD) protecting property of an ESD protecting device in a fabrication method of a semiconductor device using a self-aligned silicide **CMOS** process. The semiconductor device has a silicide blocking portion which prevents a self-aligned silicified reaction by forming a gate **electrode** on **drain** and/or source of an ESD protecting device and simultaneously forming a dummy gate electrode which is separated from the gate electrode.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

Al

L30 ANSWER 11 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2000:531634 HCAPLUS
DN 133:113704
TI Self-aligned contacts to **source/drain** silicon **electrodes** utilizing polysilicon and metal silicides
IN Lukanc, Todd
PA Advanced Micro Devices, Inc., USA
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6096644	A	20000801	US 1998-149081	19980908
	US 6291860	B1	20010918	US 2000-549930	20000414
PRAI	US 1998-149081	A3	19980908		

AB Self-aligned contacts to the source and drain regions of a **MOS** device are formed by selectively removing portions of sidewall spacers from polysilicon **source** and **drain electrodes** . Metal silicide layers are then formed in contact with the exposed polysilicon portions and extending over and in contact with resp. source and drain regions formed in a semiconductor **substrate surface**.
IT **7440-02-0, Nickel**, processes **7440-32-6, Titanium**, processes
RL: DEV (Device component use); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in fabrication of self-aligned contacts to **source/drain** silicon **electrodes** utilizing polysilicon and metal silicides)
RN 7440-02-0 HCAPLUS
CN Nickel (8CI, 9CI) (CA INDEX NAME)

Ni

RN 7440-32-6 HCAPLUS
CN Titanium (8CI, 9CI) (CA INDEX NAME)

Ti

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L30 ANSWER 12 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2000:230257 HCAPLUS
DN 132:230630
TI Manufacture of self-aligned silicide
IN Lu, Huotie; Lin, Jianting

PA Hualian Electronic Co., Ltd., Peop. Rep. China
SO Faming Zhuanli Shenqing Gongkai Shuomingshu, 17 pp.
CODEN: CNXXEV
DT Patent
LA Chinese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	CN 1195889	A	19981014	CN 1997-110284	19970410
	CN 1067804	B	20010627		
PRAI	CN 1997-110284		19970410		

AB A method for manufacturing semiconductor element comprises forming insulating layer on semiconductor **substrate**, forming polysilicon layer with lateral protrusions extending onto the **substrate** on the insulating layer, depositing metal layer on the polysilicon layer, and annealing at 600-750° to form metal silicide layer on the polysilicon **surface**. The semiconductor element may also be after-treated by etching with NH4OH/H2O2/H2O, and annealing for the 2nd time at .apprx.850°. A method for manufacturing transistor with **MOS** element comprises forming insulating layer on semiconductor **substrate**, forming polysilicon electrode with lateral protrusions extending onto the **substrate**, forming doped **source electrode/drain electrode** region on **substrate** by ion implantation by using the polysilicon electrode as mask, and forming metal silicide layer on the polysilicon electrode. The metal silicide is from the silicide of Ti, Co, Ni, Pt, or Pd.

L30 ANSWER 13 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 2000:157678 HCAPLUS
DN 132:174573
TI Forming a metal gate for **CMOS** devices using a replacement gate process
IN Huang, Jenn Ming; Su, Chi-Wen; Wu, Chung-Cheng; Chen, Shui-Hung
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6033963	A	20000307	US 1999-385523	19990830
PRAI	US 1999-385523		19990830		

AB In a method of forming a metal gate for a **CMOS** device using a replacement gate process, sidewall spacers are formed on a dummy electrode prior to forming the metal gate, allowing source and drain formation prior to metal gate formation, and a W layer is selectively deposited to act as an each or CMP stop and to reduce source and drain resistance. The process begins by forming a dummy gate oxide layer and a polysilicon dummy gate electrode layer on a **substrate** structure and patterning them to form a dummy gate. Lightly doped source and drain regions are formed by ion implantation using the dummy gate as an implant mask. Spacers are formed on the sidewalls of the dummy gate. Source and drain regions are formed by implanting ions using the dummy gate and spacers as an implant mask and performing a rapid thermal anneal. A W layer is selectively deposited on the dummy gate **electrode** and the **source** and drain regions. A blanket dielec. layer is formed over the dummy gate and the **substrate** structure. The blanket dielec.

layer is planarized by chemical mech. polishing, stopping at the W layer. The W layer overlying the dummy gate and the dummy gate are removed, thereby forming a gate opening. A gate oxide layer and a metal gate electrode layer are formed in the gate opening. The gate electrode layer is planarized to form a metal gate, stopping at the blanket dielec. layer.

IT **7429-90-5**, Aluminum, processes **7440-32-6**, **Titanium**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(forming a metal gate for **CMOS** devices using a replacement gate process)

RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

RN 7440-32-6 HCAPLUS
CN Titanium (8CI, 9CI) (CA INDEX NAME)

Ti

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L30 ANSWER 14 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1999:819137 HCAPLUS
DN 132:57990
TI Method of producing a semiconductor device
IN Ammo, Hiroaki; Miwa, Hiroyuki
PA Sony Corporation, Japan
SO Eur. Pat. Appl., 28 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 967645	A2	19991229	EP 1999-112001	19990621
	EP 967645	A3	20001025		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 2000012714	A2	20000114	JP 1998-174971	19980622
	US 6159784	A	20001212	US 1999-332038	19990614
PRAI	JP 1998-174971	A	19980622		

AB In producing a semiconductor device, the resistivities of the **base**, collector, and source/drain regions in a BiCMOS are decreased and the production step is simplified. The method comprises forming a gate electrode (a 1st semiconductor layer) on a **substrate**; forming an insulating film; forming a 2nd semiconductor layer; leaving the 2nd semiconductor layer and the insulating film on the bipolar part and removing them on the **CMOS** part to form sidewalls on the sides of the gate **electrode**; forming **source/drain** regions; forming a Ti layer over the entire **surface** and forming silicide on the **surfaces** of the 2nd semiconductor layer, the

source/drain regions, and the gate electrode; and forming a **base** electrode by patterning the 2nd semiconductor layer.

L30 ANSWER 15 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1999:551795 HCAPLUS
DN 131:164205
TI c-axis oriented thin film ferroelectric transistor memory cell and its fabrication
IN Hsu, Sheng Teng; Lee, Jong Jan; Peng, Chien Hsiung
PA Sharp Kabushiki Kaisha, Japan; Sharp Microelectronics Technology, Inc.
SO Eur. Pat. Appl., 26 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 936675	A2	19990818	EP 1998-310500	19981221
	EP 936675	A3	20010808		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	US 6011285	A	20000104	US 1998-2364	19980102
	JP 11261019	A2	19990924	JP 1998-330036	19981119
	TW 416152	B	20001221	TW 1998-87119983	19981202
PRAI	US 1998-2364	A	19980102		

AB A method of forming the c-axis FEM cell semi-conductor structure includes forming a semiconductor structure having a ferroelec. memory (FEM) gate unit on a substate of single crystal Si; forming a conductive channel of a 1st type for use as a source junction region and a drain junction region; forming a conductive channel of a 2nd type to act as a gate junction region between the source junction region and drain junction region; depositing an FEM gate unit over the gate junction region, including depositing a lower electrode, a c-axis oriented Pb5Ge3O11 FE layer and an upper electrode, in which the FEM gate unit is sized on the gate junction region such that any edge of the FEM gate unit is a distance D from the edges of the source junction region and the drain junction region, and depositing an insulating structure about the FEM gate unit. The structure of the c-axis FEM cell semiconductor includes a Si sub-state; a source junction region and a drain junction region located in the **substrate**; a gate junction region located between the source junction region and the drain junction region; a FEM gate unit including a lower electrode, a c-axis oriented Pb5Ge3O11 FE layer and an upper electrode; in which the FEM gate unit is sized on the gate junction region such that any edge of the BEM gate unit is a distance D from the edges of the source junction region and the drain junction region; an insulating layer, having an upper **surface**, overlying the junction regions, the FEM gate unit and the **substrate**; and source, **drain** and gate **electrodes**.

IT **7440-06-4**, **Platinum**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(as upper electrode in c-axis oriented thin film ferroelec. transistor memory cell and its fabrication)

RN 7440-06-4 HCAPLUS
CN Platinum (8CI, 9CI) (CA INDEX NAME)

Pt

L30 ANSWER 16 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1999:551792 HCAPLUS
DN 131:164202
TI Partial silicidation method to form shallow source/drain junctions in semiconductor devices such as **MOS** transistors with low leakage currents
IN Maa, Jer-Shen; Hsu, Sheng Teng; Peng, Chien-Hsiung
PA Sharp Kabushiki Kaisha, Japan; Sharp Microelectronics Technology, Inc.
SO Eur. Pat. Appl., 19 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 936664	A2	19990818	EP 1999-300474	19990122
	EP 936664	A3	20000419		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	US 6071782	A	20000606	US 1998-23383	19980213
	TW 400557	B	20000801	TW 1998-87119337	19981121
	JP 11251591	A2	19990917	JP 1998-338212	19981127
	US 6218249	B1	20010417	US 1999-455588	19991206
PRAI	US 1998-23383	A	19980213		

AB A process of forming silicide at uniform rates across the entire source/drain region is provided. A two-step annealing method permits the thickness of the silicide formed on the edge of a Si electrode to be substantially the same as it is in the center of the electrode. A 1st, low temperature anneal begins the salicidation process across the **source /drain electrode surface**. The time and temperature are controlled so that the metal is only partially consumed. The annealing is interrupted to remove excess silicidation metal, especially the unreacted metal overlying oxide areas neighboring the Si electrode. Then, the silicidation is completed at a higher temperature anneal. Because the excess metal was removed, the resulting silicide layer is uniformly flat, permitting the transistor to be fabricated with shallow junction areas and low leakage currents. In one embodiment of the invention, the crystalline structure of source and drain **surfaces** is annihilated before the deposition of metal, to lower annealing temps. and add precise control to the silicidation process. A transistor having a uniformly thick silicide layer, fabricated in accordance with the above-mentioned method, is also provided.

IT **7440-02-0, Nickel**, processes **7440-06-4, Platinum**, processes **7440-32-6, Titanium**, processes **7440-47-3, Chromium**, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); RCT (Reactant); REM (Removal or disposal); PROC (Process); RACT (Reactant or reagent); USES (Uses)
(in partial silicidation method to form shallow source/drain junctions in semiconductor devices such as **MOS** transistors)
RN 7440-02-0 HCAPLUS
CN Nickel (8CI, 9CI) (CA INDEX NAME)

Ni

RN 7440-06-4 HCAPLUS
CN Platinum (8CI, 9CI) (CA INDEX NAME)

Pt

RN 7440-32-6 HCAPLUS
CN Titanium (8CI, 9CI) (CA INDEX NAME)

Ti

RN 7440-47-3 HCAPLUS
CN Chromium (8CI, 9CI) (CA INDEX NAME)

Cr

L30 ANSWER 17 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1999:457971 HCAPLUS
DN 131:81571
TI Sub-micron metal gate **MOS** transistor and its fabrication
IN Hsu, Sheng Teng; Nguyen, Tue; Evans, David R.
PA Sharp Kabushiki Kaisha, Japan; Sharp Microelectronics Technology, Inc.
SO Eur. Pat. Appl., 13 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 929105	A2	19990714	EP 1999-300130	19990108
	EP 929105	A3	19991222		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	US 6274421	B1	20010814	US 1998-4991	19980109
	JP 11224949	A2	19990817	JP 1998-336093	19981126
	TW 434901	B	20010516	TW 1998-87120673	19981211
PRAI	US 1998-4991	A	19980109		

AB A **MOS** transistor is formed on a single-crystal Si **substrate** doped to form a conductive layer of a 1st type, and includes: an active region formed on the **substrate**; source and drain regions located in the active region, doped to form conductive channels of a 2nd type; a metal gate region <1 μm wide located in the active region between the source and drain regions; a gate oxide region located over the gate region; an oxide region located over the structure; and source, gate, and **drain electrodes**, each connected to their resp. regions, and each made of a combination of a contact metal and an electrode metal. An alternate embodiment includes a pair of **MOS** transistors with interconnected gate **electrodes** and **drain electrodes**.

IT **7429-90-5**, Aluminum, processes **7440-50-8**, **Copper**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical

process); PROC (Process); USES (Uses)
(contacts containing; in fabrication of sub-micron metal gate **MOS** transistors)
RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

RN 7440-50-8 HCAPLUS
CN Copper (7CI, 8CI, 9CI) (CA INDEX NAME)

Cu

L30 ANSWER 18 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1999:440125 HCAPLUS
DN 131:66589
TI Fabrication of self-aligned metal silicide films on a **MOS** transistor structure
IN Chee, Lay; Naem, Abdalla
PA National Semiconductor Corp., USA; National Semiconductor Corp.(N.D.Ges.D.States Delaware), Santa Clara
SO Ger. Offen., 8 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 19857037	A1	19990708	DE 1998-19857037	19981210
	DE 19857037	B4	20041230		
	US 5966607	A	19991012	US 1997-1531	19971231
PRAI	US 1997-1531	A	19971231		

AB In the fabrication of salicide layers on a **MOS** transistor structure with decreased risk of forming silicide bridges between the **source/drain electrodes** and the polysilicon gate electrode, unidirectional ion metal plasma deposition is used to form a metal layer on a **surface** of the **MOS** transistor structure, so that the ratio of the thickness of the metal layer on the gate sidewall spacer to the thickness of the metal layer on the polysilicon gate electrode is ≤0.2. The relatively thin metal layer on the gate sidewall spacer decreases the probability of formation of metal silicide defects.
IT **7440-02-0, Nickel**, processes **7440-06-4, Platinum**, processes **7440-32-6, Titanium**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabrication of self-aligned metal silicide films on a **MOS** transistor structure containing)
RN 7440-02-0 HCAPLUS
CN Nickel (8CI, 9CI) (CA INDEX NAME)

Ni

RN 7440-06-4 HCAPLUS
CN Platinum (8CI, 9CI) (CA INDEX NAME)

Pt

RN 7440-32-6 HCAPLUS
CN Titanium (8CI, 9CI) (CA INDEX NAME)

Ti

L30 ANSWER 19 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1998:761717 HCAPLUS
DN 130:19652
TI Nonvolatile semiconductor memory device having memory cell transistor provided with offset region acting as a charge carrier injecting region
IN Sakagami, Eiji; Naruke, Kiyomi
PA Kabushiki Kaisha Toshiba, Japan
SO U.S., 15 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5838041	A	19981117	US 1996-720618	19961002
	JP 09097849	A2	19970408	JP 1995-254782	19951002
	JP 09252059	A2	19970922	JP 1996-60621	19960318
	JP 3630491	B2	20050316		
PRAI	JP 1995-254782	A	19951002		
	JP 1996-60621	A	19960318		

AB The present invention **discloses** a nonvolatile semiconductor memory device having a memory cell transistor in which an offset region is provided as a charge carrier injecting region. An insulating film and a gate electrode is formed in order of mention on a semiconductor **substrate**. Source/drain regions are formed on the **surface** of the semiconductor **substrate** with the gate electrode interposed there between. The drain has an LDD (Lightly Doped Drain) structure. Also, a layered film of Si oxide films and a SiNx film is provided on a channel region between an edge of the gate **electrode** and a **source** diffusion layer. To be more specific, the layered film is formed in such a way that the SiNx film is interposed between the Si oxide films, constituting a side wall of the gate electrode. The SiNx film is a charge carrier accumulating layer. Contact holes are formed in an insulating film between layers, resp. reaching the source and drain regions. Each of the contact holes are filled with a conductive material (contact plug). A conductive barrier film (diffusion protecting film) is provided on the bottom and to the inner wall portions of the contact hole. The contact plugs resp. connect the source and the drain to upper layer, Al wiring.

IT **7429-90-5**, Aluminum, uses

RL: DEV (Device component use); USES (Uses)
(nonvolatile semiconductor memory device having memory cell transistor provided with offset region acting as charge carrier injecting region)
RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L30 ANSWER 20 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1998:719101 HCAPLUS
DN 129:338784
TI Raised silicided **source/drain electrode** formation with reduced **substrate** silicon consumption
IN Maa, Jer-shen; Hsu, Shen Teng
PA Sharp Microelectronics Technology Inc., USA; Sharp Kabushiki Kaisha
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5830775	A	19981103	US 1996-756782	19961126
PRAI US 1996-756782		19961126		

AB A method is provided for forming silicided **source/drain electrodes** in active devices in which the electrodes have very thin junction regions. Silicidation material is deposited on a **wafer** and rapid-thermal-annealed at a temperature and for a time calculated to produce metal-rich or Si-deficient silicide on the electrodes. The metal-rich or Si-deficient silicide is selectively formed on the semiconductor electrodes and not on oxide or other insulating **surfaces**. A selective etch removes the silicidation material which has not reacted with Si, including metal overlying insulating **surfaces**. Then, after cleaning the silicide **surfaces**, a layer of Si is deposited over the structure and a 2nd rapid thermal anneal is performed at a higher temperature than the 1st rapid thermal anneal. In the 2nd rapid thermal anneal, addnl. Si from the deposited Si layer is incorporated into the silicide, converting it from metal-rich or Si-deficient silicide into the more stable disilicide phase. Upon removal of any unconsumed silicide, the disilicide contacts are completed. The process can be controlled to produce ultrathin junction depths of <500 Å with overlying silicide contacts ≤1000 Å thick. The result is the formation of thermally stable silicide contacts which are self-aligned with the electrodes.

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L30 ANSWER 21 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1998:579945 HCAPLUS
DN 129:224471
TI Manufacture of semiconductor devices
IN Nagashima, Naoki
PA Sony Corp., Japan

SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 10233371	A2	19980902	JP 1997-35143	19970219
PRAI JP 1997-35143		19970219		

AB The title process comprises (1) formation of a refractory metal film only on regions on a Si **substrate** by self-alignment for formation of electrodes, and selective formation of a metal film only on the silicide film and (2) formation of sidewalls on sides of the gate electrode, formation of a etching-resistant layer on the entire **surface** of the **substrate** and selective removal thereof to expose an insulating film on the gate electrode while covering the device isolation film, etching removal of the insulating film exposing a Si polycryst. film of the gate electrode, removal of the etching-protective film, doping of the source-drain regions and the Si gate electrode using the side walls and the device isolation film as a mask, deposition of a refractory metal on the entire **surface** and heat treatment forming silicide films on the Si gate **electrode** and the **source**-drain regions, and selective formation of a metal film on the silicide layers. The metal film has no contact with the semiconductor **substrate** and no reaction with Si of the **substrate**.

L30 ANSWER 22 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1998:392133 HCAPLUS
DN 129:35240
TI Fabrication of a sub-half micron **CMOS** transistor
IN Loh, Ying-tsong; Ding, Lily
PA VLSI Technology, Inc., USA
SO U.S., 20 pp., Cont. of U. S. Ser. No. 417,638, abandoned.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5759901	A	19980602	US 1997-905234	19970801
PRAI US 1995-417638	B1	19950406		

AB A technique for forming a high-performance sub-half micron **MOS** transistor is **disclosed** which has improved short channel characteristics without degradation of device performance. The transistor comprises a semiconductor **substrate**, a gate **electrode**, graded **source** and drain impurity regions, a 1st set of gate sidewall spacers, and a 2nd set of gate sidewall spacers. The graded source and drain impurity regions comprise a relatively linear continuum of doped regions, ranging from lightly doped (LDD) regions, to moderately doped (MDD) regions, to heavily doped regions. Addnl., the transistor may include a punch-through barrier region located within the **substrate** under the gate electrode. With these features, the transistor allows for more precise control of conductive channel length without degradation of either (1) body factor and current drive, and/or (2) junction leakage, without compromising hot carrier immunity.
RE.CNT 18 THERE ARE 18 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L30 ANSWER 23 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1996:751377 HCAPLUS
DN 126:41327
TI Manufacture of semiconductor device with low-electric resistance gate **electrode** and **source drain**
IN Inoe, Akira; Sekine, Makoto; Watanabe, Hirohito; Pponma, Ichiro
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08274043	A2	19961018	JP 1995-72801	19950330
	US 5661052	A	19970826	US 1996-617686	19960319
PRAI	JP 1995-72801	A	19950330		

AB The title manufacture involves the following steps: (1) forming a gate pattern consisting of a lower amorphous- or polycryst. Si layer and an upper layer; (2) forming the 1st Si3N4 side-walls on the side **surfaces** of the gate pattern; (3) forming the 2nd SiO2 side-walls on the 1st Si3N4 side-walls; (4) by exposing the upper layer of the gate pattern to HF steam under reduced pressure, removing the upper layer of the gate pattern to form a space surrounded by the side-walls and the lower amorphous- or polycryst. Si layer of the gate pattern; (5) forming source/drain region; and (6) selectively forming a high m.p. metal or high m.p. metal silicide on the source/drain regions and on the lower amorphous- or polycryst. Si layer exposed in the space. The upper layer of the gate pattern may be a PSG or BPSG layer. The 2nd SiO2 side-walls prevent flow of H3P04 from the gate pattern to the source/drain or field oxide films.

IT **7440-02-0, Nickel**, processes **7440-06-4, Platinum**, processes **7440-32-6, Titanium**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(manufacture of semiconductor device with low-elec. resistance gate **electrode** and **source drain**)
RN 7440-02-0 HCAPLUS
CN Nickel (8CI, 9CI) (CA INDEX NAME)

Ni

RN 7440-06-4 HCAPLUS
CN Platinum (8CI, 9CI) (CA INDEX NAME)

Pt

RN 7440-32-6 HCAPLUS
CN Titanium (8CI, 9CI) (CA INDEX NAME)

Ti

L30 ANSWER 24 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1996:724071 HCAPLUS
DN 126:41255
TI Manufacture of silicon semiconductor apparatus
IN Gohara, Hiromi; Miura, Hideo; Nishimura, Asao; Ando, Norio; Fujii, Juji; Fujita, Masahiro; Kobayashi, Yoshihisa
PA Hitachi Ltd, Japan; Hitachi Tokyo Electronics
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08255769	A2	19961001	JP 1995-59360	19950317
	JP 3270985	B2	20020402		
PRAI	JP 1995-59360		19950317		

AB In the manufacture involving (1) accumulating a Ni film on a Si **wafer**, and (2) heating the Ni film and the Si **wafer** for allowing to react them to form a Ni silicide layer; the Si **wafer** is heated at 100-300°, when accumulating the Ni film. In a **MOS** transistor on a Si **wafer**, a Ni silicide layer between its source (or **drain**) and an **electrode** wiring, a Ni silicide layer between a polycryst. Si gate electrode and a Ni film is formed by the method. Silicidation of Ni proceeds smoothly to form stable Ni silicide layer having excellent elec. contact.

IT **7440-32-6, Titanium,** uses
RL: DEV (Device component use); USES (Uses)
(conductor; manufacture of silicon semiconductor apparatus having **nickel** silicide layer)
RN 7440-32-6 HCAPLUS
CN Titanium (8CI, 9CI) (CA INDEX NAME)

Ti

IT **7440-02-0, Nickel,** uses
RL: DEV (Device component use); RCT (Reactant); RACT (Reactant or reagent); USES (Uses)
(conductor; manufacture of silicon semiconductor apparatus having **nickel** silicide layer)
RN 7440-02-0 HCAPLUS
CN Nickel (8CI, 9CI) (CA INDEX NAME)

Ni

L30 ANSWER 25 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1996:718743 HCAPLUS
DN 125:344988
TI Semiconductor devices and electroluminescence driving circuits
IN Ueno, Juji; Uno, Toshihiko; Kuroishi, Yoshitaka
PA Matsushita Electronics Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.

CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 08250662	A2	19960927	JP 1995-49536	19950309
PRAI JP 1995-49536		19950309		

AB The title devices have a high-withstand voltage horizontal n-ch **MOS** transistor comprise stretched n-type drain/source regions and Al **source electrodes** formed on a p-type Si **substrate**, and **drain** and gate **electrodes**. The **drain electrode** and bonding pads are connected via spiral polycryst. Si film which is elec. connected to the Al **drain electrode** via an insulative contact window. The polycryst. Si film and the bonding pad are elec.-connected by lamination. The arrangement gives the **MOS** transistors a high-ON resistance without decrease of the drain saturated current.

IT **7429-90-5**, Aluminum, properties
RL: DEV (Device component use); PRP (Properties); USES (Uses)
(**source/drain electrode**; semiconductor devices and electroluminescence driving circuits)
RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

L30 ANSWER 26 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1996:688867 HCAPLUS
DN 125:345130
TI Insulated gate field effect transistor semiconductor apparatus and its manufacture
IN Yamazaki, Shunpei; Mase, Akira
PA Handotai Energy Kenkyusho, Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 08242003	A2	19960917	JP 1995-335551	19951222
JP 2652364	B2	19970910		
PRAI JP 1995-335551		19951222		

AB The transistor apparatus comprises an Al gate electrode having an Al oxide layer coating at least on side face of the gate electrode, an interlayer insulating film having a contact hole (at the edge of the Al oxide layer on side wall of the gate electrode) for pullout **electrode** for the **source**- and drain regions, and an electrode wiring. The manufacture involves the following steps; (1) forming a semiconductor islander region on a **substrate** having an insulating **surface**, (2) forming an Al gate electrode on the semiconductor region through the gate insulating film, (3) implanting an impurity into the semiconductor region using the gate electrode as a mask, (4) anodic oxidizing the gate electrode to form an oxide layer at least on the side face of the gate

electrode, (5) forming an interlayer insulating film on the semiconductor region, (6) forming a contact hole for pullout electrode in the interlayer insulating film, and (7) forming an electrode wiring. The device shortened distance between the channel region and the source/drain regions.

IT **7429-90-5**, Aluminum, uses
RL: DEV (Device component use); RCT (Reactant); RACT (Reactant or reagent); USES (Uses)
(gate electrode; manufacture of insulated gate field effect transistor)

RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

L30 ANSWER 27 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1996:179191 HCAPLUS
DN 124:248000
TI High-pressure-resistant **MOS** transistors
IN Shindo, Masao
PA Matsushita Electronics Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08008423	A2	19960112	JP 1994-140166	19940622
PRAI	JP 1994-140166		19940622		

AB The transistors comprise a channel between a gate **electrode** and a **drain electrode** on a semiconductor **substrate** and part of the drift region on the channel **surface**. The **MOS** transistors are highly integrated and have high pressure resistance.

IT **7429-90-5**, Aluminum, uses
RL: DEV (Device component use); USES (Uses)
(**drain electrode**; high-pressure-resistant **MOS** transistors)

RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

L30 ANSWER 28 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1995:975447 HCAPLUS
DN 123:356672
TI **Metal-oxide-semiconductor** device with a **substrate** contact structure.
IN Endou, Kazuo
PA Kabushiki Kaisha Toshiba, Japan
SO Eur. Pat. Appl., 10 pp.
CODEN: EPXXDW

DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 676815	A1	19951011	EP 1995-105114	19950405
	EP 676815	B1	19990630		
	R: DE, FR, GB				
	JP 07283414	A2	19951027	JP 1994-66832	19940405
	US 5929488	A	19990727	US 1996-764274	19961212
PRAI	JP 1994-66832	A	19940405		
	US 1995-416203	B1	19950404		

AB Formed on a grounded semiconductor **substrate**, over an insulation layer, is a semiconductor layer of the same conductivity type as the **substrate**. Formed on the semiconductor layer are source and drain regions of the opposite conductivity type from the **substrate**. The drain region is formed so that it reaches the insulation layer. A gate insulation film is formed on the semiconductor layer and a gate electrode is formed on the gate insulation film and between the source and drain regions. A conductive member is embedded in a through hole formed from a portion of the semiconductor layer to the semiconductor **substrate** through the insulation layer. A **source electrode** is formed so that the conductive member in the through hole and the source region are connected to each other by means of the **source electrode**. A **drain electrode** is connected to the drain region. A common-source **MOS** device is thus formed without a wiring to ground the source by means of the conductive member embedded in the through hole that connects the **source electrode** to the grounded semiconductor **substrate**.

IT **7429-90-5**, Aluminum, uses
RL: DEV (Device component use); USES (Uses)
(**MOS** device having **substrate** contact structure containing)

RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

L30 ANSWER 29 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1995:605646 HCAPLUS
DN 122:328253
TI Contact structure and method for connecting a circuit element to a silicon **substrate** and memory cells using it
IN Evans, Joseph Tate, Jr.; Bullington, Jeff Allen
PA Radiant Technologies, Inc., USA
SO PCT Int. Appl., 15 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9508187	A1	19950323	WO 1994-US8681	19940728
	W: AU, CA, JP, KR				
	RW: AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				

	AU 9474784	A1	19950403	AU 1994-74784	19940728
PRAI	US 1993-123289	A	19930917		
	WO 1994-US8681	W	19940728		

AB A capacitor can be formed over the source of a transistor. A cell is constructed by 1st constructing a **CMOS** transistor having a drain, a gate region consisting of gate oxide and a gate **electrode**, and a **source**. The gate structures are insulated with a glass layer. A capacitor is then constructed by depositing a bottom **electrode** on the **source**. A ceramic layer is then deposited and sintered. Finally, the top electrode is deposited. The resulting structure may be heated in the presence of O to >800° without destroying the elec. connection between the Si **substrate** and components connected to a Pt conductor. The invention uses a TiN or TiW barrier layer to connect the Pt conductor to the Si **substrate**. The barrier layer is deposited as a single crystal on the Si **substrate**. The Pt layer is then deposited on the barrier layer. The region of the Pt layer in contact with the barrier layer is also a single crystal.

IT **7440-06-4, Platinum**, uses
RL: DEV (Device component use); USES (Uses)
(elec. contacts to silicon **substrates**)

RN 7440-06-4 HCAPLUS
CN Platinum (8CI, 9CI) (CA INDEX NAME)

Pt

L30 ANSWER 30 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1995:276934 HCAPLUS
DN 122:44237
TI **MOS** transistors with high breakdown voltage
IN Mishima, Takeshi
PA Yokogawa Electric Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 06151832	A2	19940531	JP 1992-303713	19921113
PRAI JP 1992-303713		19921113		

AB Semiconductor **substrates** (e.g., Si) with buffer oxide films are selectively oxidized with masks to form field oxide films and bird's beaks for isolating device domains, the masks and buffer oxide films are removed, gate oxide films are formed in the same places, gate electrodes covering the gate insulator films and extending over the bird's beaks are formed, impurity ions are implanted in the **substrates** using masks (e.g., Al) covering the gate **electrodes** to form **source** and drain regions, and the impurities are thermally diffused to create pn junctions reaching the bird's beak bottom.

IT **7429-90-5**, Aluminum, uses
RL: NUU (Other use, unclassified); USES (Uses)
(masks for ion implantation in silicon **substrates** for **MOS** transistors)

RN 7429-90-5 HCAPLUS

CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

L30 ANSWER 31 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1994:643578 HCAPLUS
DN 121:243578
TI Manufacture of complementary **MOS** (**metal-oxide** -insulator) **semiconductor** device
IN Oda, Munetaka
PA Kawasaki Steel Co, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 06204420	A2	19940722	JP 1992-349603	19921228
PRAI JP 1992-349603		19921228		

AB The title method involves the following steps; forming an element-separating film on a semiconductor **substrate**, forming a gate oxide film, a Si gate **electrode**, and a **source**-drain region on the both sides of the electrode, chemical vapor depositing a Si oxide film on the whole **surface**, anisotropic etching to remove the Si oxide film other than on the sidewall of the gate electrode and the upper part of the sidewall of the element-separating film, laminating a metal film of Ti, Co, or Ni on the whole **surface**, and heating to form a silicide film selectively on the upper part of the source-drain region and the gate electrode. The device showed controlled threshold voltage.
IT **7440-02-0**, **Nickel**, processes **7440-32-6**, **Titanium**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(polycide structure in manufacture of **CMOS** semiconductor device)
RN 7440-02-0 HCAPLUS
CN Nickel (8CI, 9CI) (CA INDEX NAME)

Ni

RN 7440-32-6 HCAPLUS
CN Titanium (8CI, 9CI) (CA INDEX NAME)

Ti

L30 ANSWER 32 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1994:619479 HCAPLUS
DN 121:219479
TI Bipolar complementary **MOS** device
IN Furuhata, Tomoyuki

PA Seiko Epson Corp., Japan
SO U.S., 14 pp. Cont. of U.S. Ser. No. 691,448, abandoned.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5336911	A	19940809	US 1992-975129	19921112
	EP 341821	A3	19900926	EP 1989-303391	19890406
	EP 341821	B1	19950927		
	R: DE, FR, GB, NL				
	US 5059549	A	19911022	US 1990-499906	19900327
PRAI	JP 1988-111421	A	19880510		
	US 1989-329561	B1	19890328		
	US 1991-691448	B1	19910425		

AB A BiCMOS device having a bipolar device and a plurality of **MOS** devices is formed on a principal **surface** of a semiconductor **substrate**. The device includes a plurality of element isolation regions, each composed of a 1st semiconductor region formed in the **substrate** and having the same conductivity type as the **substrate** , a thick dielec. layer formed on the 1st semiconductor region, an emitter electrode and/or a collector electrode formed in the bipolar device, gate electrodes formed in the **MOS** devices, a low-resistivity polycryst. Si layer with a buried contact forming the **source** or **drain electrode** of the **MOS** devices, and a high-resistivity polycryst. Si layer connected to the low-resistivity polycryst. Si layer.

L30 ANSWER 33 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1993:684206 HCAPLUS
DN 119:284206
TI Complementary bipolar-complementary **MOS** devices and their manufacture
IN Uga, Kimiharu; Honda, Hiroki; Ishida, Masahiro; Ishigaki, Yoshiyuki
PA Mitsubishi Denki K.K., Japan
SO Ger. Offen., 36 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 4230858	A1	19930819	DE 1992-4230858	19920915
	JP 05226589	A2	19930903	JP 1992-29555	19920217
	US 5319234	A	19940607	US 1992-916666	19920722
PRAI	JP 1992-29555	A	19920217		

AB In the device, the **base** electrode of an npn bipolar transistor and the **drain electrode** of a **PMOS** transistor are made of the same polycryst. semiconductor, the **base** electrode of a pnp bipolar transistor and the **drain electrode** of an **NMOS** transistor are made of the same polycryst. semiconductor, and the **source electrodes** of the **PMOS** and **NMOS** transistors are made of Al wiring. The device makes possible good elec. conductivity of the **source electrodes**, size reduction of the **drain electrodes** , and simplification of the process steps in preparation of the **base** electrodes, so that the size of the devices can be decreased with simple

process steps without decreasing the elec. conductivity
IT **7429-90-5**, Aluminum, uses
RL: DEV (Device component use); USES (Uses)
(**source electrodes** from, in complementary bipolar and **MOS** devices)
RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

L30 ANSWER 34 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1993:566857 HCAPLUS
DN 119:166857
TI Gas sensor for ambient air
IN Sato, Yasuhiro; Tanigawara, Shinji; Oota, Wasaburo; Yamaguchi, Takayuki; Manaka, Junji; Takano, Shigeki
PA Ricoh Kk, Japan; Ricoh Seiki Co Ltd
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 05052790	A2	19930302	JP 1991-242718	19910828
PRAI JP 1991-242718		19910828		

AB Noxious gases in ambient air are rapidly determined by using the elec. resistance change of **metal oxide semiconductive** membrane sputtered on the ceramic **base** plate of a sensor. The sensor comprises 2 oppositely-arranged coil-shaped electrodes, an elec. heater, and means for supplying elec. **source** to the **electrodes**. The semiconductive membrane is preferably the metal oxide of Sn, Ti, In, W, Ni, Cd, and Zn, and has a thickness of 0.05-5 μm. In one embodiment, an ultrafine particle interlayer containing Si3N4, MgF2 or Ta2O5 is placed between the semiconductive membrane and the ceramic **base** plate. The sensor is durable and has high accuracy.

L30 ANSWER 35 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1993:507354 HCAPLUS
DN 119:107354
TI Manufacture of semiconductor device having contact part
IN Shimonishi, Yasuyuki
PA Seiko Epson Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 05109648	A2	19930430	JP 1991-272765	19911021
PRAI JP 1991-272765		19911021		

AB The device, having a **MOS** transistor, a resistor, etc. on a semiconductor **substrate**, is manufactured by forming a gate wiring and

a **source-drain electrode**, forming an interlayer insulating film, opening a contact-hole, forming a thin elec. conducting layer, etching the conducting layer except in the contact-hole, embedding the contact-hole with a polycryst. or amorphous Si, etching off the Si except in the contact-hole, implanting p- or n-type impurity ions into plug polycryst. or amorphous Si in the contact-hole, and forming a metal wiring layer. The device showed low contact resistance.

IT **7429-90-5**, Aluminum, uses
RL: USES (Uses)
(wiring, leveled, in manufacture of semiconductor device)

RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

L30 ANSWER 36 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1992:624462 HCAPLUS
DN 117:224462
TI Erasable and programmable random-access memories
IN Takenaka, Kazuhiro
PA Seiko Epson Corp., Japan
SO PCT Int. Appl., 15 pp.
CODEN: PIXXD2
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9206500	A1	19920416	WO 1991-JP1346	19911004
	W: US				
	RW: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LU, NL, SE				
	JP 04144282	A2	19920518	JP 1990-267602	19901005
	EP 504425	A1	19920923	EP 1991-917336	19911004
	R: DE, FR, GB, IT, NL				
PRAI	JP 1990-267602	A	19901005		
	WO 1991-JP1346	W	19911004		

AB In an erasable and programmable ROM, in which capacitors using a ferroelec. substance are integrated with a semiconductor **substrate**, particularly in the structure of memory-forming unit cells, the top electrode of the capacitor is connected, through a wiring **electrode**, with the **source** diffusion layer of an **MOS** transistor. The drain diffusion layer of the transistor is connected with a 1st wiring electrode containing, e.g., Al as its main component, while the other electrode of the capacitor acts as a 2nd wiring electrode. A 3rd wiring electrode containing, e.g., Al as its main component is placed in parallel with the 2nd wiring electrode, and connected with the 1st wiring electrode directly or through the 2nd wiring electrode. The ROM is suited for large-scale integration and capable of fast operation.

IT **7429-90-5**, Aluminum, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(wiring electrodes from, for capacitors, erasable and programmable ROMs containing)

RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

A1

L30 ANSWER 37 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1992:502394 HCAPLUS
DN 117:102394
TI Semiconductor memory device and manufacture thereof
IN Igarashi, Takashi; Mori, Haruhisa
PA Fujitsu K. K., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 04063472	A2	19920228	JP 1990-175847	19900703
PRAI JP 1990-175847		19900703		

AB A semiconductor memory device (e.g., mask ROM) has multiple **MOS** memory transistors, in which writing data can be effected by depressing channel regions by using ion implantation. This semiconductor memory device comprises device isolation regions and metal interconnections which function as ion-implantation mask. The manufacture comprises the steps of: (1) forming field oxide films on a semiconductor **substrate**; (2) forming gate oxide films; (3) forming gate **electrodes**; (4) forming **source** and drain regions by using ion implantation; (5) forming an interlayer insulating film on the overall **surface**; (6) forming contact holes in the interlayer insulating film, and depositing a metal film on the overall **surface**; and (7) patterning the metal film remained on and along the field oxide films, and thereby forming metal interconnections which function as ion-implanting masks.
IT **7429-90-5**, Aluminum, properties
RL: PRP (Properties)
(interconnection and mask, manufacture of ROM from)
RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

A1

L30 ANSWER 38 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1987:416321 HCAPLUS
DN 107:16321
TI Semiconductor device
IN Takabayashi, Seiichiro; Sakata, Masanori; Yadoiwa, Yoshiaki
PA NEC Corp., Japan
SO Jpn. Tokkyo Koho, 3 pp.
CODEN: JAXXAD
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI	JP 62014941	B4	19870404	JP 1979-78485	19790621
	JP 56002638	A2	19810112		
PRAI	JP 1979-78485	A	19790621		

AB A method for fabricating a moisture-resistant semiconductor device (e.g., Si-gate **MOS** large-scale integrated circuit) involves the following steps: (1) forming source and drain regions in a semiconductor **substrate** having field and gate oxide films and gate electrodes; (2) covering the field oxide film, gate **electrodes**, and **source** and drain regions with a high-concentration phosphosilicate-glass layer and then with an oxide film (0.2-1.5 μm) containing P2O5 1-7 mol%; (3) heat treating to make the oxide film more dense; (4) forming an Al interconnection connected to the source and drain regions; and (5) covering the overall **surfaces** with a vapor-deposited film.

IT **7429-90-5**, Aluminum, uses and miscellaneous
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(elec. interconnections, insulators for, in semiconductor devices)

RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

L30 ANSWER 39 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1986:217678 HCAPLUS
DN 104:217678
TI Semiconductor device
IN Takeuchi, Hiroshi
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PI	JP 61005580	A2	19860111	JP 1984-126175	19840619
	EP 171864	A1	19860219	EP 1985-300047	19850104
	EP 171864	B1	19890419		
	R: DE, FR, GB				
	US 4616401	A	19861014	US 1985-690302	19850110
PRAI	JP 1984-126175	A	19840619		

AB A method for fabricating a semiconductor device (e.g., **MOS** devices) involves the following steps: (1) forming a gate electrode on the element region surrounded by a field insulator film of a semiconductor **substrate** via a gate insulator film; (2) doping with an impurity to prepare source and drain regions; (3) selectively forming an insulator film on the sides of the gate electrode; (4) selectively forming a conductor film on the gate **electrode**, **source** and **drain** regions, and their surrounding regions; (5) forming an insulator film having contact holes on the overall **surfaces**; and (6) forming an electrode interconnection. Optionally, the conductor may be comprised of a chemical-vapor-deposited metal or metal silicide film.

IT **7429-90-5**, uses and miscellaneous
RL: DEV (Device component use); TEM (Technical or engineered material

use); USES (Uses)
(conductor films, for semiconductor devices)
RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

L30 ANSWER 40 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1984:16297 HCAPLUS
DN 100:16297
TI Silicon-on-sapphire **MOS** devices
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 58151057	A2	19830908	JP 1982-32740	19820302
PRAI JP 1982-32740		19820302		

AB Smooth-**surfaced** Si-on-sapphire **MOS** devices with low interfacial leakage currents are formed by: (1) epitaxy of Si on sapphire, (2) double ion implantation of O using a SiO2 mask to give peak O concns. at the **surfaces** and interfaces, (3) heating at 1000° in N2 to convert the O layers to SiO2, (4) removing the mask, and (5) forming gates, **sources**, **drains** and **electrodes**.
IT **7429-90-5**, uses and miscellaneous
RL: DEV (Device component use); USES (Uses)
(elec. contacts from, for silicon-on-sapphire **MOS** devices)
RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

L30 ANSWER 41 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1981:630746 HCAPLUS
DN 95:230746
TI **MOS**-type semiconductor device
PA Cho LSI Gijutsu Kenkyu Kumiai, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 56111263	A2	19810902	JP 1980-10198	19800131
PRAI JP 1980-10198	A	19800131		

AB A **MOS** semiconductor device is obtained by depositing an insulator film on a semiconductor **substrate** (e.g., from Si) with gate-**electrode**, **source**, and **drain** regions,

opening contact holes in the insulator film, depositing an interconnection-forming film (e.g., from Al) and pos. resist (e.g., from PMMA) on the entire **surface**, and exposing the resist to charged-particle beams or x-ray irradiation to form interconnections with a pattern which covers the gate-electrode regions. The variation of the gate threshold voltage is prevented, which is caused by electron traps formed in the gate-electrode region during the exposure.

IT **7429-90-5**, uses and miscellaneous
RL: USES (Uses)
(elec. interconnections from, for **MOS** with low gate-threshold-voltage variation)

RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

L30 ANSWER 42 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1973:509630 HCAPLUS
DN 79:109630
TI High frequency field effect transistor
PA Philips Electronic and Associated Industries Ltd.
SO Brit., 7 pp.
CODEN: BRXXAA
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	GB 1322511	A	19730704	GB 1970-43149	19700909
	NL 6913958	A	19710316	NL 1969-13958	19690912
	CH 506888	A	19710430	CH 1970-506888	19700909
	SE 363542	B	19740121	SE 1970-12274	19700909
	AT 7008170	A	19760815	AT 1970-8170	19700909
	AT 336081	B	19770412		
	FR 2061685	A5	19710625	FR 1970-32896	19700910
	FR 2061685	B1	19740322		
PRAI	NL 1969-13958	A	19690912		

AB The frequency-dependent output characteristics of a common **metal -oxide-semiconductor** field-effect transistor are considerably improved by extending the Al **source electrode** contact zone to contact the **substrate** at the **surface**, thus shorting out the pn junction between source and **substrate**. The nonrectifying properties of this short enabled higher signal frequencies (≥107 Hz) to be employed.

IT **7429-90-5**, uses and miscellaneous
RL: TEM (Technical or engineered material use); USES (Uses)
(transistors, containing short-circuited layer of, for high-frequency operation)

RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

L30 ANSWER 43 OF 43 HCAPLUS COPYRIGHT 2005 ACS on STN
AN 1970:72418 HCAPLUS
DN 72:72418
TI Ohmic contact to a semiconductor body
PA RCA Corp.
SO Brit., 7 pp. Division of Brit. 1177381
CODEN: BRXXAA
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	GB 1177382		19700114		
PRAI	US		19660224		

AB A method is described for making improved ohmic contact to a semiconductor body and is particularly applicable to integrated circuits of the monolithic semiconductor type and to circuits which include complementary pairs of **MOS** (**metal-oxide-semiconductor**) transistors. The method basically comprises subjecting that portion of the **surface** of the body at which contact is to be made to an ionic **discharge** in an inert gas, removing the inert gas, and depositing a metal on the treated **surface** portion under high-vacuum conditions. In the process of manufacturing an integrated circuit, after covering the unit **surface** with photoresist, openings are etched through to expose the source and drain **surfaces** of the two **MOS** transistors. The unit is placed in a vacuum chamber which is provided with **discharge** electrodes. The chamber is pumped down to 10-2 mm Hg and back-filled with Ar to a pressure of 50 μ. A p.d. of 800 V d.c. is then placed across the **discharge** electrodes and the unit **surfaces** subjected to a glow **discharge** for 1-30 min at room temperature This modifies the exposed source and drain **surfaces** such that better adherence of Al, which is to be used as a contact metal, is obtained. The **discharge** is stopped, the Ar removed from the chamber, and the chamber is pumped down to a high vacuum. Al metal is then evaporated over the entire **surface**, forming a layer 1500 g thick. The Al forms an ohmic contact layer over the source and drain regions and also covers the remainder of the circuit area, from which it is removed. This procedure is repeated with the addnl. step of heating the unit to 550 ° in N for 3 min to cause alloying of the Al on the **source** and **drain electrodes** to the Si. After alloying, the p-type transistor has a typical conductivity, Gm, of 600-800 microomhs at 1 mA of drain current and a threshold voltage, Vth, of -4.5 to -6.5 V. Without the heating step, units have a typical Gm of 100 at 0.5mA and a Vth of -9 to -11 V.

IT **7429-90-5**, uses and miscellaneous
RL: DEV (Device component use); USES (Uses)
(elec. contacts, to silicon, **surface** treatment in elec. **discharge** prior to deposition of)
RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al